We claim:

1. A semiconductor device in chip format, comprising:

a chip;

electrical connection pads disposed on said chip;

at least one first insulating layer disposed on said chip such that said electrical connection pads are free of said first insulating layer on at least one surface;

interconnects running on said first insulating layer and in each case lead from said electrical connection pads to base regions;

a second insulating layer disposed on said interconnects and on said first insulating layer, said second insulating layer being thicker than said first insulating layer, said second insulating layer have openings formed therein and each of said openings leads to a respective one of said base regions;

cylinders made of a cured, elastic conductive adhesive material disposed in each of said openings;

small plastic balls having a metallic coating on an outside disposed in each case on a respective one of said cylinders

made of said cured, elastic conductive adhesive material in a region of a free end of each of said openings.

2. The semiconductor device according to claim 1, wherein said second insulating layer is at least four times thicker than said first insulating layer.

3. A method for producing semiconductor devices in a chip format, which comprises:

providing chips;

placing electrical connection pads on the chips;

applying at least one first insulating layer to at least one surface of the chips such that the electrical connection pads are left at least partially uncovered by the first insulating layer;

producing interconnects on the at least one first insulating layer, the interconnects leading to base regions of external connection elements;

applying a second insulating layer on the interconnects and on the at least one first insulating layer, the second insulating layer being thicker than the first insulating layer;

forming openings in the second insulating layer above the base regions;

introducing a conductive adhesive into the openings and the conductive adhesive having a cylinder shape in the openings;

placing small plastic balls having a metallic coating on the outside onto the conductive adhesive in a region of a free end of each of the openings; and

curing the conductive adhesive.

4. The method according to claim 3, which comprises using a doctor blade for introducing the conductive adhesive into the openings.

5. The method according to claim 3, which comprises

forming the chips on a wafer; and

after the curing of the conductive adhesive step, dividing the wafer to obtain the semiconductor devices.

6. A method for producing semiconductor devices in a chip format, which comprises the steps of:

providing chips;

placing electrical connection pads on the chips;

applying at least one first insulating layer to at least one surface of the chips such that the electrical connection pads are left at least partially uncovered by the first insulating layer;

producing interconnects on the at least one first insulating layer, the interconnects leading to base regions of external connection elements;

applying a second insulating layer on the interconnects and on the at least one first insulating layer;

forming openings in the second insulating layer above the base regions;

introducing a conductive adhesive into the openings;

placing small plastic balls having a metallic coating on the outside onto the conductive adhesive in a region of a free end of each of the openings; and

curing the conductive adhesive.

7. The method according to claim 6, which comprises introducing the conductive adhesive into the openings using a doctor blade.

8. The method according to claim 6, which comprises:

forming the chips on a wafer; and

after the curing of the conductive adhesive, dividing the wafer to obtain the semiconductor devices.

9. A method for producing a semiconductor device in a chip format, which comprises the steps of:

providing chips;

placing electrical connection pads on the chips;

applying at least one first insulating layer to at least one surface of the chips such that the electrical connection pads are left at least partially uncovered by the first insulating layer;

producing interconnects on the at least one first insulating layer, the interconnects leading to base regions of external connection elements;

applying a second insulating layer on the interconnects and on the at least one first insulating layer;

forming openings in the second insulating layer above the base regions;

introducing solder paste into the openings;

placing metallized small plastic balls onto the solder paste in a region of a free end of each of the openings; and

remelting the solder paste.

10. The method according to claim 9, which comprises introducing the solder paste into the openings using a doctor blade.

11. The method according to claim 9, which comprises:

forming the chips on a wafer; and

after the remelting of the solder paste step, dividing the wafer to obtain the semiconductor devices.